Senior Project – Electrical Engineering and English Double Major – 2019

Designing a Low-Cost Ultrasound Pulser/Receiver

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Introduction:

- Ultrasound imaging is an incredibly powerful technology that grants the ability to see inside a patient or subject without cutting them open
- Professor Buma has a very expensive ultrasound pulser/receiver (~$2000) that he uses for such imaging
- He would like to be able to replicate this machine but for less money
- The final device should have the same basic functionality as the high-cost one, but may have less adjustable features
- The final device will be mounted on a PCB and have a metal housing

Goals for Fall Term:

- Obtain SRG funding
- Create and run simulations of the pulser/receiver
- Construct a working prototype
  - Design and test each stage of the pulser/receiver
    - Design pulser circuitry first
    - Begin receiver work once pulser works properly
- Plan how to implement input adjustments
- Define Winter Term goals

Current Work:

- Designing and testing breadboarded digital logic pulser circuit

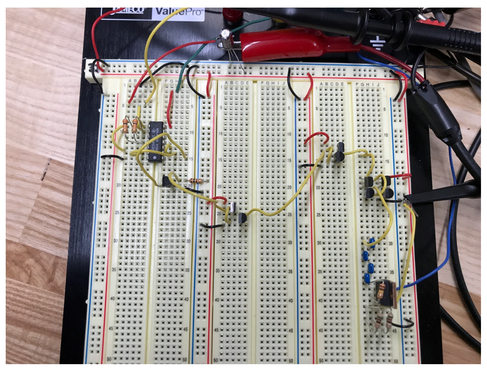

Figure 5: Breadboarded digital logic pulser circuit

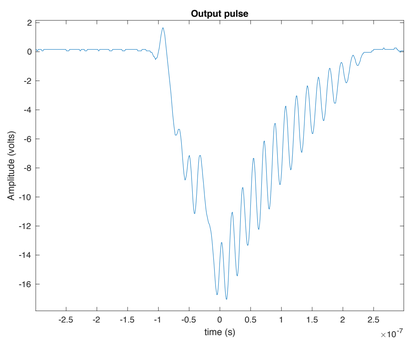

Figure 6: Final Output of Digital Logic Pulser Circuit

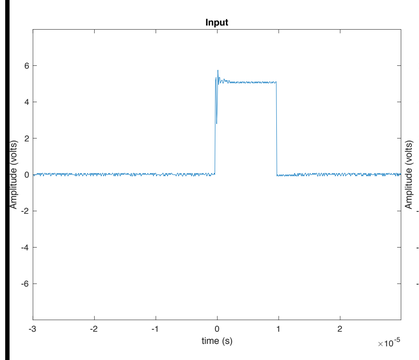

Figure 7: Digital Logic Input Pulse

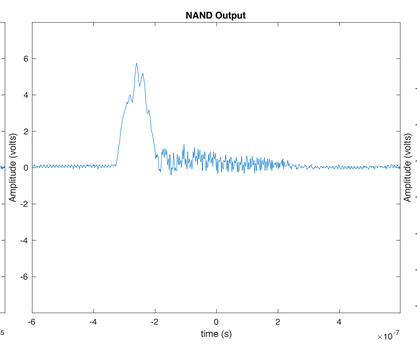

Figure 8: Output of NAND Logic Stage

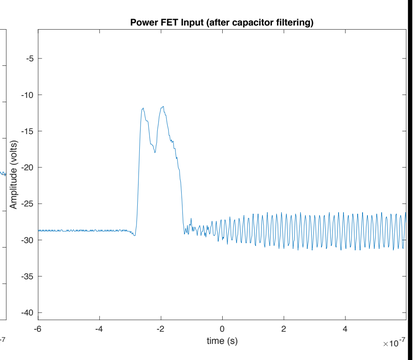

Figure 9: Input of High-Power MOSFET

- Between the inverter output and the NAND input, resistors are necessary in order to "slow down" the pulse switch time, so the NAND gate is high at different, but overlapping times
- Next steps are to attempt to remove the large ripple from the output
- Will begin soldering components to see if they help reduce ripple
- Researching components for purchase, including a high-voltage power supply to create high-voltage pulses, and components that can withstand said high voltages

Completed Work:

- Ran simulation based on Jeremy A. Brown and Geoffrey R. Lockwood's paper (used different MOSFETs than they had indicated)

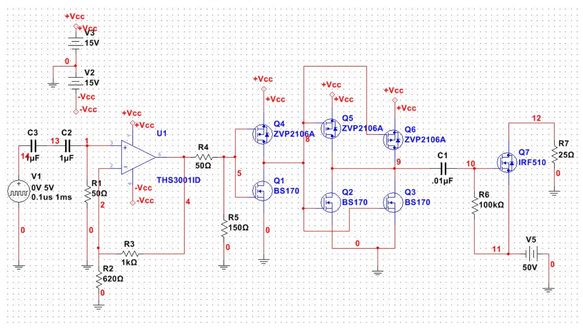

Figure 1: Multisim Schematic of Brown and Lockwood's Design

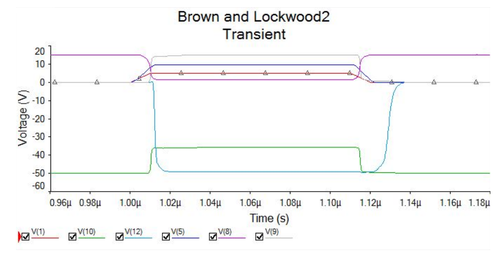

Figure 2: Input, Stage Outputs, and Final Output of Brown and Lockwood's Design

- The output pulse width is dependent upon the input pulse width
- The op amp increases the voltage so the MOSFETs receive a high enough gate voltage for the p-channel to turn on
- Each MOSFET pair acts as a push-pull (each stage inverts the signal)
  - The second pair is in parallel, and increases the total current the high-power MOSFET receives (also inverting the received signal)
- The input is the red line, above in Figure 2, and the final output is the light blue line shown above in Figure 2
- When consulting with Professor Buma, he mentioned that he did not want the input pulse width to affect the output pulse width
- He then suggested using digital logic to replace the op-amp, relying on the transience of the NAND gate to produce the final output voltage

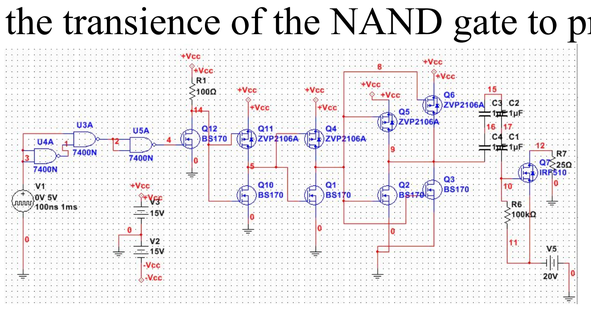

Figure 3: Multisim Schematic of Digital Logic Design

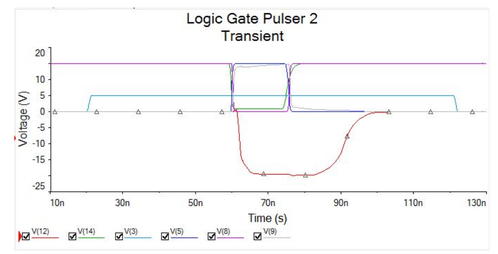

Figure 4: Input, Stage Outputs, and Final Output of Digital Logic Design

- This design includes a single n-channel MOSFET to increase the NAND output current (which also inverts the signal, requiring the addition of another push-pull stage)
- This design is identical to the breadboarded design I have
- The final output pulse width is smaller than the design in Figure 1
- In Figure 4, the input is shown in light blue and the final output in red

Future Work:

- Finish testing the pulser output and solder an early prototype
- Design, test, and solder the receiver circuit
- Begin designing and testing adjustable input conditions
- Lay out components using a PCB software
- Design a case and housing for the final product
- Assemble the finished product

Acknowledgements:

- Thanks to Union College, Professor Buma, Gene Davison, and coffee