Designing a Low-Cost Ultrasound Pulser/Receiver

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ECE-498: Capstone Design Report

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1. INTRODUCTION

Ultrasound imaging is an incredibly powerful, useful technology. It allows for medical practitioners and those studying living beings to see inside a patient or subject without having to cut them open or otherwise harm them. This process allows for real-time images to be taken, making it easy for doctors to diagnose and researchers to find what they are attempting to observe. However, while this technology can be incredibly beneficial to those attempting to utilize it, the machines used to create and receive ultrasound pulses can be incredibly complex, allowing for very precise, fine-tuned adjustment of the output signal, and therefore expensive. Although this degree of function is often desired, as it can produce better, higher quality images, it is not often necessary. Professor Buma currently owns an ultrasound machine that costs approximately $2,000. He is able to use it for his research, but sometimes he requires more than one ultrasound device. At the price of the industry machine, purchasing many would not be cost-efficient. Though the manufactured device is very high-functioning, he sometimes does not require as high a degree of functionality as it can provide. An image of the industry machine is shown below in Figure 1 [1].

Figure 1: Image of the Industry Machine this Project is Attempting to Replicate

Therefore, the problem this project sets out to solve and a solution to said problem become obvious. This project is focused on designing a low-cost pulser/receiver for use with an ultrasound transducer. While it will not have all the high-level functions of the original device, it

will have all of the base functionality, most obviously the ability to output a high voltage pulse and receive a low voltage input. Some input adjustments are also desired, such as the ability to change the repetition rate or trigger type. Because this project sets out to create a practical, low-cost alternative to the industry machine, one large secondary requirement is cost—the project must be able to be constructed using a limited budget. Because Professor Buma could potentially require the use of more than one of these low-cost devices, the design should also be fairly easy to replicate. The design should also be fairly adaptable, so that components can be replaced with ease. This will allow for future improvements to be made upon the device.

Ultrasound pulses are generated by connecting an ultrasound transducer to a pulser circuit, and received by connecting an ultrasound transducer to a receiver circuit. The pulser circuit generates a very high voltage pulse with negative amplitude, which drives the transducer. The receiver circuit is designed for much lower voltages, and must be able to receive signals on the scale of millivolts (mV). In the case of this project, the pulser circuit output and receiver circuit input will be connected to the same ultrasound transducer through a coaxial cable. This introduces another layer of complexity, as the receiver circuitry must be isolated from that of the pulser. The goal of this project is to design the pulser/receiver, which will then be connected to an ultrasound transducer through a coaxial cable. A rough sketch of the intended operation of the final device is shown below in Figure 2.

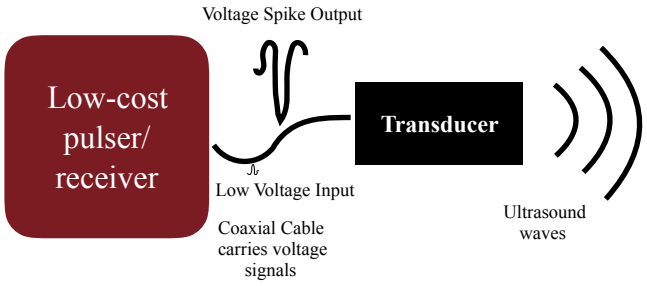

Figure 2: High-Level Sketch of Key Device Stages

The project will be designed in stages. The focus of the Fall Term was the pulser circuitry, with additional research being done into overall functionality and components. Preliminary research into the receiver circuitry was also completed. The receiver circuitry and the input adjustments will be the primary focus of the Winter Term. The overall device will also be planned and designed during the Winter Term. Eventually, each separate stage of the project will be combined into one single device that will plug into the wall outlet. The testing of this final device will be the focus of the remainder of the Winter Term, as well as the completion of the final report and presentation.

The remainder of this report includes the following. Section two features background information on the topic and device. Section three provides more detail about the design requirements, including a block diagram of individual stages. Section four details design alternatives, and includes a component justification. Section five discusses the design currently being prototyped. Section six focuses on some preliminary results from the prototype design. Section seven is a potential project implementation schedule for the upcoming winter term. Section eight provides a list of all references used throughout this report. Section nine is comprised of various appendices referenced throughout the report.

2. BACKGROUND

2.1. Previous Research and Study

Because this project is largely constrained by cost, and because the final device will be a somewhat less functional version of a widely available machine, there has not been a great deal of work done to find low-cost alternatives to the existing industry unit. One major investigation conducted about this particular problem was done by Jeremy A. Brown and Geoffrey R. Lockwood, but their study focused only upon the pulser circuitry and assumed that components such as the high voltage power supply and ultrasound transducer had already been purchased, and so did not factor these component costs into their budget [2]. Therefore, while their circuit appears to be fairly inexpensive, this project will also have to include the price of components necessary to the overall device that were not included in their paper. The need for both pulses out and reflections in to be transmitted along the same co-axial cable introduces the need for protection circuitry, as discussed by Jens Kristian Poulsen [3]. This paper examines various techniques that can be used to isolate the high voltage output pulse from the low voltage received, justifying the design and use of each individual technique.

Beyond the cost element, the paper by Brown and Lockwood discusses several other aspects and constraints of designing an ultrasound pulser. The amplitude of the pulse depth is dependent upon the voltage supply used to drive the power MOSFET. However, that pulse depth is also dependent upon the speed of the high-power MOSFET, to a degree as is the pulse width. They observed excess ringing immediately following the high-voltage pulse, but found it to be fairly negligible in comparison to the magnitude of the high-voltage pulse.. They also offered solutions to isolate the ringing if it was absolutely necessary to isolate the pulse from all excess

ringing. In their testing, they did not attempt to drive a load higher than 100 ohms (Ω), though they did find that it was possible to drive capacitive loads. The final prototype of their design could be used for ultrasound imaging purposes ranging from 1 to 60 megahertz (MHz) [2]. Their design is below in Figure 3.

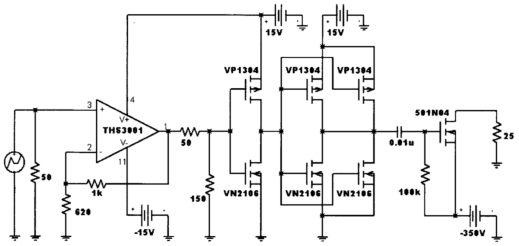

Figure 3: Brown and Lockwood's Pulser Circuit Schematic

Their design is quite simple, and was easy to simulate and prototype, though there were several further constraints not discussed in the paper itself. These constraints include the dependence of the output pulse width on the input pulse width and the difficulty in outputting the appropriate amplitude from the op-amp sub-phase to turn the P-channel MOSFET fully on. As both of these characteristics are necessary in order for the device to function properly, these are major constraints to Brown and Lockwood's design that this project will attempt to remedy.

Since the pulser signal must be isolated from the receiver signal, it is also important to study and gain an understanding of protection circuitry. Poulsen discusses the use of diodes in order to ensure that the pulse signal is isolated from the receive signal. A diode expander is connected to the pulser circuitry, allowing the high voltage pulse out, but preventing the receive pulse from returning into the pulser. Similarly, a diode limiter is connected before the pre-amplification stage of the receiver circuitry in order to allow the low voltage received pulse to reach the amplifier while preventing the high pulser voltage from reaching or destroying the receiver circuitry. This can be implemented with a capacitor, a 50 Ω resistor for impedance

matching, or a transformer. Poulsen argues that the transformer is the best option, since it isolates the protection circuitry components from the initial high voltage pulse and provides better electrical matching between the transducer and the receiver circuitry [3]. The chosen protection circuitry is shown below in Figure 4.

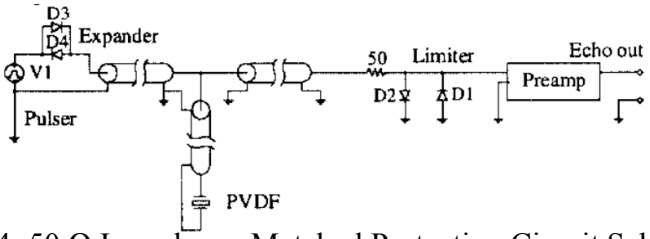

Figure 4: 50 Ω Impedance-Matched Protection Circuit Schematic

While the transformer protection circuit offers the most benefit, due to time constraints, the easier to implement 50 Ω impedance-matched option will be chosen.

One paper that discusses receiver circuitry for an ultrasound transducer is by L. Svilainis and V. Dumbrava. The pre-amplifier phase they design is meant to be used with ultrasound waves propagating through air, and closely examines the signal, the noise, and the signal to noise ratio (SNR). Through their work, they isolate some of the factors heavily involved in producing a great deal of noise. They also posit a few solutions to reducing noise, each dependent upon the parameter contributing the most to the noise. They note that their solution will not work for all ultrasound transducers, but they do provide a preliminary circuit that works with relatively low source impedance transducers [4]. The circuit they designed is shown in Figure 5, below.

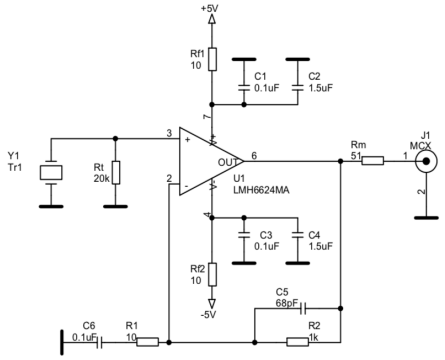

Figure 5: Preliminary Design of Pre-Amplification Stage of Receiver

Based upon the results they have achieved, new component values can be calculated and an appropriate pre-amplification circuit designed. The signal, noise, SNR, and other factors will have to be closely examined in order to begin these calculations.

2.2. Potential Project Impacts

The successful completion of this project would have a large positive impact on Professor Buma and his research. Even if he does not pursue replication of the project, having at least one additional ultrasound pulser/receiver with all necessary base functionality will allow him to image an additional subject without having to buy a new, more expensive machine. The more successful the project is—the more high-level functions added to the overall design—would only continue to make this positive impact greater, as it would allow for more functionality or more precise imaging. Because the final design is expected to be fairly simple, it should also be easily replicable, meaning that should Professor Buma decide that one additional ultrasound device is not suitable for his needs, he should be able to quickly and easily construct another device, potentially even being able to alter some of the optional features to provide more or less functionality as appropriate.

While Professor Buma is the target of the project's positive impact, the low-cost design could also aid others who are interested in inexpensive ultrasound imaging solutions. There are surely other professors here at Union who rely heavily upon ultrasound imaging when conducting their research who could be positively impacted by the existence of a low-cost alternative to more expensive machines. The final design will be well labeled and easy to pick up and use, even for those unfamiliar with circuitry. This is a large factor in the final design, as the final device should function similarly to the industry machine in that it should be self-contained,

with the only connections extending to power, the input/output cable, and an external trigger. If it is externally similar to the industry machine, it will be easy for anyone familiar with the proper operation of that device to use the final device created through this project.

Regardless of the state of the final project, it can also aid future students in learning more about how ultrasound pulsers and receivers work. Students can study the final design itself if they are interested in learning more about practical applications of circuit design, but can also easily repeat the design and conduct their own tests and improvements upon it. Depending upon the level of additional features, this project could be expanded or improved upon by future capstone students. Because of the many individual functionality improvements, it is very easy to add additional features to the final design, as well as remove other features.

There should be no ethical issues associated with the deign or use of this project. Because ultrasound imaging is often conducted on living beings, it should be safe to use and pose no threat of electrical shock to either the user or the subject. Legally, it should comply with the same codes and standards as the industry machine. So long as care is taken to isolate the high voltage supply and other dangerous concerns, the final device should be able to comply with these standards easily.

3. DESIGN REQUIREMENTS

In order for this device to be considered successful and functional, it must meet a series of design requirements, which are outlined below. Most of these requirements were defined based upon Professor Buma's requests, as he is the target customer of the final device. The requirements are broken up into three categories: requirements that apply only to the pulser, requirements that apply only to the receiver, and requirements that apply to the overall system.

3.1. Design Requirements for Pulser Stage

The pulser stage is the primary focus of the project, as its requirements will have the greatest impact on the overall device. There are two levels of requirements, those that are absolutely necessary for the device to work, and those that are desired for higher levels of functionality, but not absolutely necessary to the device's basic functionality. The high-level requirements are still strongly desired by the customer, but not meeting them will not mean the project as a whole has failed.

3.1.1. Base Requirements for Pulser Stage

The pulser stage includes a set of requirements that are necessary in order to ensure basic functionality of the overall system. Most importantly, the pulser must be able to create a negative voltage spike of at least 150 V. The width of this pulse should be approximately 20 nanoseconds (ns). The repetition rate of the output pulse shall be approximately 1 kHz. An external trigger is required so the device is informed about when to output a pulse. When the device receives this trigger, it should be able to output the negative voltage spike. The external trigger will operate on a 0-5 volt logic scale, so the pulser should be designed to receive a 5 volt input. The output load of the pulser, the ultrasound transducer, can be modeled with an

impedance of approximately 50 Ω. The output of the pulser will also be connected to the receiver circuitry, also designed for an output impedance of 50 Ω. When the pulser is on, these two loads will appear to be in parallel, making 25 Ω an appropriate choice to model the pulser behavior of the final device during pulser-only testing phases.

3.1.2. High-Level Requirements for Pulser Stage

After basic functionality is confirmed, additional functions will be added and tested to the overall circuitry. These additional functions are primarily input adjustments, changes that can be made before any signal has been sent to the device, that will affect the final shape or behavior of the output pulse. The repetition rate shall be adjustable, ideally up to 20 kHz, but 5-10 kHz would be considered an acceptable value. An option for an internal trigger that would keep time and trigger the device without additional input is also highly desired.

3.2. Design Requirements for Receiver Stage

The biggest concern related to the receiver circuitry is the shared connection to the coaxial cable connected to the ultrasound transducer. The transducer requires a very high voltage pulse to transmit ultrasound waves, but will return a comparatively very low voltage signal to the device. The receiver must be protected from the pulser's output spike but still be able to detect the very low voltage reflected back to the device. The signal returned by the transducer will be on the scale a few mV, and must be amplified so that it can be viewed on an oscilloscope or other signal visualizer.

3.3. Design Requirements for Overall Device

Like the pulser, the final device has some basic requirements and some requirements that are not absolutely necessary to the device's overall function but desired by the customer. Unlike

the case of the pulser, however; not meeting these requirements can severely limit the final functionality of the device, so while they are higher level requirements, they should also be met.

3.3.1. Base Requirements for Overall Device

Though it is not a technical requirement, one very important overall requirement of the device's design is cost. As the device is supposed to be a low-cost alternative, it should not be cost-prohibitive to construct. The device is also limited by the Student Research Grant program; the project has been approved for a $399 budget. The original SRG proposal and award letter are attached in Appendices A and B.

The high voltage output means that electrical safety must be paid careful attention to, so the current flowing through and the power dissipated by the device do not cause harm to the user. The current flow and power dissipation must be closely monitored in order to ensure the safety of both the user and the subject. The device should be able to meet all the standards of electrical safety that the industry machine can.

The final device shall behave like Professor Buma's more expensive machine, meaning that it will run off the AC wall line and have the appropriate BNC input/output connections. It should be of similar dimensions and weight, though there are no specific size and weight constraints on the device.

3.3.2. High-Level Requirements for Overall Device

The device's circuitry shall be implemented through the use of a Printed Circuit Board (PCB). The use of a PCB will allow for ease of repeatability, should Professor Buma desire to replicate the device. The use of a PCB would also make for faster connections, and therefore a more stable output pulse. This is a future concern, but it will improve the functionality greatly.

The device should ultimately be mounted on a metal housing or similar casing, with appropriate input and output connections. The size of this final device should not be much larger than the original machine, which is 7 inches wide by 3.5 inches tall by 9.1 inches long, but the physical size of the device is not an immediate concern [1].

4. DESIGN ALTERNATIVES

Several different components were chosen for this project, and some are still in the process of being decided upon. The pulser components are essentially finalized, as are some of the overarching components. The receiver components have not yet been finalized, but the general parts necessary have been determined. This section is broken up similarly to the previous section, with each subsection detailing the parts most relevant to the design.

4.1. Component Alternatives and Justifications

Many alternatives were considered, and in some cases tested, before they were ultimately decided against. The most specific design is the pulser circuit, as the general design has been finalized. The specific components must be replaced and tested for optimization. The receiver circuit has been designed with a general idea of necessary parts, and several overall components are currently being chosen. This section is broken up by these three categories in order to distinguish which parts are most relevant to which phase of the design.

4.1.1. Pulser Design Component Alternatives and Justifications

The pulser circuit was originally constructed based upon Brown and Lockwood's paper, using the parts available within the ECBE department. This meant that the op-amp was lower powered and slower, the power MOSFET could not handle the same current, and the other MOSFETs had different ratings. Instead of the THS3001 op-amp [5] suggested by the paper [2], the breadboarded prototype was constructed using an LF356N [6]. Instead of the 501N04A power MOSFET [7], the prototype was constructed using an IRF510 [8]. While the BS170 N-channel MOSFET [9] was not the same as the one suggested by the paper, the VN2106 [10], they had similar characteristics, and therefore using alternate components should not have a large

effect on the overall design. The P-channel MOSFET available for use, the VP2106 [11], was the same as the one suggested by the paper, and functioned as expected when paired with the BS170 N-channel MOSFET.

Minimal testing was done on this prototype, but during these tests, it was observed that the output pulse width was dependent upon the input pulse width. This is because using an op-amp only amplified the input pulse's amplitude, but did nothing to change the width. Since Professor Buma desired the final output width to be fixed, this design could not be used. Therefore, the SN74HC00N high-speed 4-gate NAND chip [12] was used instead, as the pulse width could be set by taking advantage of the inherent propagation delay of digital logic. This high-speed chip was chosen over its lower-speed counterpart in order to limit the propagation delay caused by the logic chip. This produced the desired final pulse width behavior, with the final pulse width being dependent upon the value of the delay resistor. While the final pulse width is not yet at 20 ns, it is no longer reliant upon the input pulse width.

Because both the VN2106 and the BS170 N-channel MOSFETs have similar characteristics [9] [10] and the VP2106 P-channel MOSFET can be replaced with other MOSFETs with similar characteristics, it was determined that the final choice of MOSFET for the push-pull switch was not largely important, so long as the MOSFETs could achieve the desired behavior. The deciding factor in this case will be cost, and since the ECBE department has multiple BS170s and often uses VP2106s, these will be the components used for the push-pull switches. The push-pull stages are not incredibly demanding on the overall system, nor do they require a high voltage, current, or power tolerance, so the choice to use the BS170 and VP2106 MOSFETs will not have a great effect on the overall circuit performance [9] [11].

The final power MOSFET is incredibly important, as it allows for the high voltage pulse to be output. If it cannot react quickly enough or withstand the high power dissipated across it, the final output pulse will not behave as expected and the overall device could even malfunction or break. The 501N04A chosen by Brown and Lockwood is rated at 500 V, 4.5 A, and has turn-on and turn-off times of 4 ns each [7]. Their paper discussed a design meant to handle -350 V and greater, but since the maximum voltage that will be dissipated across this power MOSFET is only around -150 V, the power MOSFET used does not have to be withstand such a high voltage rating. The most important factor in the choice of the power MOSFET is the turn-on and turn-off times, as these are what will affect the output pulse the most. The 201N09A power MOSFET has a turn-on time of 4 ns and a turn-off time of 4 ns, and is rated for 200 V and 9 A, making it more than sufficient for this application [13].

4.1.2. Receiver Design Components and Justifications

The receiver design consists of the protection circuitry and pre-amplification stage. The protection circuitry will consist of 2 diodes, each of which must be able to withstand the brief, approximately 3 ampere (A) current caused by the high voltage pulse. This current was calculated by using the magnitude of the high voltage pulse, 150 V, and the characteristic impedance of the pulser circuitry, 50 Ω. This current will be a major factor in the determination of several parts beyond just the protection diode. The impedance-matching resistors must also be able to withstand the power dissipation caused by the 3 A pulse. The diodes are the most important, however; since if the protection circuitry fails, the receiver circuitry can be damaged by the very high voltage and associated power dissipation. This sub-phase of the design will likely see the highest power dissipation, and the final design must account for those constraints.

The receiver pre-amplification circuitry makes use of an op-amp to amplify the noise received from the ultrasound transducer. The way that this op-amp is applied will drastically change the overall performance of the receiver circuitry. Svilainis and Dumbrava warn against excessive amounts of DC bias, suggesting that the amplifier feedback loop be broken in order to eliminate the problem of DC bias voltage [4]. This pre-amplification phase does not provide a great deal of amplification on its own, but it successfully removes a great deal of the signal noise from the received signal. This less noisy signal can then be passed to a proper amplification stage, also consisting of an op amp, in order to examine the received signal.

4.1.3. Overall Design Component Alternatives and Justifications

The biggest task of the Fall Term was determining an appropriate high voltage power supply. This high voltage power supply also had the majority of the SRG budget devoted to it. The original SRG proposal included an unregulated DC power supply unit by Acopian [14]. This model was designed to plug into the wall and deliver a semi-steady single output voltage. This was ultimately decided against because the unregulated nature of the supply meant that there would not be a constant voltage level delivered to the source of MOSFET, but a varied value averaging the advertised value of the power supply, which would not be conducive to a consistent pulse depth or width. After this power supply was decided against, research was conducted into on-board power supplies. One was found that was fairly small in size, but it had no means to quickly deliver a large amount of current in a short amount of time [15]. Because of this limitation of the otherwise appropriate supply, it was ultimately decided that the power supply need not be an on-board module. Studying the Acopian models again, a regulated high voltage DC power supply was found. This model can output 150 V and 100 mA [16]. While the

use of this model is not as ideal as having an on-board connection, it will be much easier to incorporate this into the overall design, especially when time constraints are taken into account.

The overall device will be powered by a +15 V wall line adapter. This voltage will be used to power the majority of the device, save for the high voltage pulse output. This value will have to be adjusted for the NAND gate chip, as it takes +5 V to power the chip [12]. The push-pull switches and the receiver circuitry will all be powered directly by the +15 V source.

5. DESIGN

The overall device has four distinct phases, each with several sub-phases. These phases are detailed in the block diagram shown in Figure 6, below. The input adjustments mostly cover the high-level requirements discussed in Section 3. The focus of this term was obtaining SRG funding, building and modifying Brown and Lockwood's pulser circuit, and testing the new pulser design. The receiver circuitry has not yet been fully designed, and only some preliminary research into the overall design has been conducted. Each phase of the design has its own section, which will discuss various aspects of the current design and potential future steps. The pulser design phase is also broken up into subsections, each discussing different design phases.

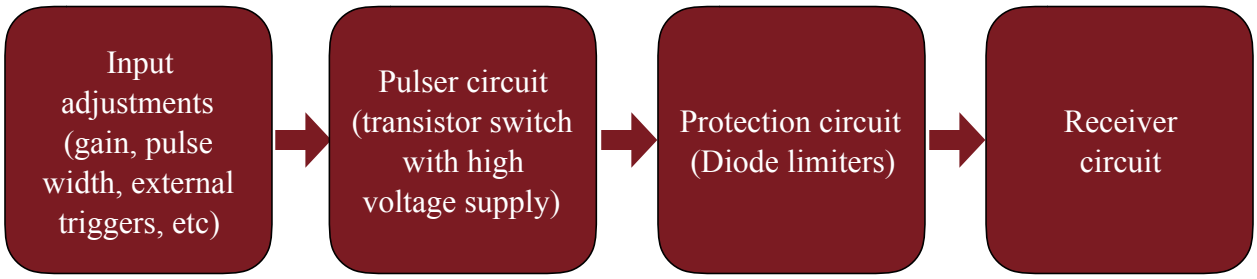

Figure 6: Block Diagram of Overall Device (Following Signal Path)

5.1. Pulser Design

During the Fall Term, the pulser design went through three distinct design and pseudo testing phases. Firstly, the circuit proposed by Brown and Lockwood was constructed and cursorily tested. Some modifications were made to that circuit, which resulted in the current circuit design. A breadboarded version of this circuit was constructed and tested more fully than the preliminary design. The preliminary results of this phase were presented during Week 9 of the Fall Term. This poster presentation is included in Appendix C. Since then, that same circuit has been soldered on a perfboard in order to create a very basic prototype of the pulser circuit.

5.1.1. Brown and Lockwood's Design

Brown and Lockwood's design consisted of three phases, detailed by the block diagram below, in Figure 7. The circuit itself is discussed in Section 2, and shown in Figure 3.

Figure 7: Block Diagram of Brown and Lockwood's Circuit

The circuit was constructed using the available parts in the ECBE department, which meant that the final circuit would not be as functional as the one described in the paper. However, this preliminary construction was enough to begin constructing the pulser circuit and considering alternative designs. A final output pulse was never achieved with this design, and no oscilloscope traces were saved before the breadboarded circuit was altered to implement digital logic. A key flaw in this design that lead to the consideration of other pulse generator options was the dependence of the output pulse width on the input pulse width.

5.1.2. Breadboarded Digital Logic Circuit

The digital logic pulser circuit can be broken down into four distinct phases. A block diagram of these phases is shown below in Figure 8.

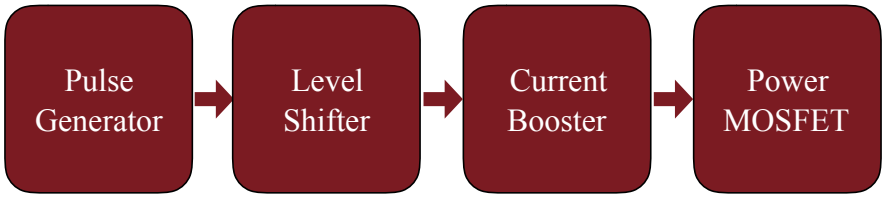

Figure 8: Block Diagram of Digital Logic Pulser Circuit

The additional phase, as compared to the previous design, is the level shifter, which is necessary to ensure that the output of the NAND logic phase is a high enough input voltage for the push-

pull MOSFET phase. Because the level shifter inverts the signal again, an additional inverting push-pull stage is also necessary. Figure 9, below, is an image of this breadboarded circuit.

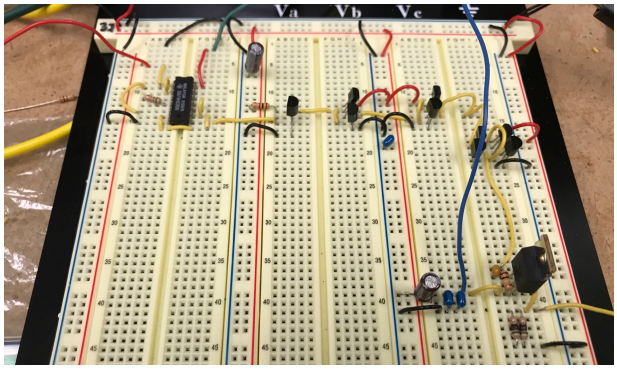

Figure 9: Breadboarded Digital Logic Circuit

Professor Buma suggested the use of digital logic gates. This meant that the amount of time the output of any given logic gate was high could be controlled by the inherent propagation delay of digital logic. A NAND gate was chosen because this implementation required inverting the signal at various stages. Because of how NAND logic works, tying the inputs of a NAND gate together functionally acts as an inverter.

The input pulse signal is fed into three pins of the SN74HC00N NAND chip—pins 1, 2, and 5. Pins 1 and 2 are connected to the same NAND gate, considered as Gate 1 by the datasheet [12]. and therefore simply invert the input signal. This inversion stage is used to introduce more delay. The output of Gate 1, pin 3 is tied to the input of Gate 2, pin 4. Theoretically, the delay caused by this inversion should produce a noticeable difference in “high” level time and cause the pulse width at the output of Gate 2, pin 6, to be much shorter than the original input pulse.

However, the propagation delay of this inversion is not long enough to produce a noticeable overlap in signal “high” levels. During breadboard testing, a resistor was introduced between pins 3 and 4 in order to “slow down” the signal response. This should cause the input signal to pin 4 to dissipate more slowly than a direct connection, meaning that the input pins to

Gate 2, pins 4 and 5, will see a more noticeable overlap in “high” times, causing the final output of Gate 2, located at pin 6, to be shorter than the input pulse, but still detectable and able to be carried forward. This signal should be a negative voltage pulse of around 5 V and 20 ns.

Pin 6 is then connected to pins 10 and 11, the input pins to Gate 4. This stage is necessary in order to make the final output of the NAND gate pulse generator phase a positive voltage pulse. The final output of the NAND gate pulse generator should be a positive voltage pulse of around 5 V and 20 ns.

This output voltage is then delivered to the gate of the BS170 N-channel MOSFET. Using a 100 Ω resistor between +15 V V_{CC} and the source allowed for the 5 V at the gate to turn on the MOSFET, causing the source voltage to reach the 15 volt output level required for later circuit phases. Because this level shifter uses a MOSFET, it also inverts the signal.

The current booster phase consists of two inverting push-pull MOSFET switches connected in series. Each stage consists of a BS170 N-channel MOSFET and a VP2016 P-channel MOSFET. The gates of the N-channel and P-channel MOSFETs are tied to each other, as are the drains. The input signal is fed into the gates, and the output signal is measured from the drains. The source of the N-channel MOSFET is connected to ground, while the source of the P-channel MOSFET is connected to the positive supply, +15 V V_{CC}, as the N-channel MOSFET was in the previous level shifting phase. These first two stages are used to increase signal stability and marginally decrease signal width. The first push-pull stage produces a positive output, and the second produces a negative output. This negative output is then connected to a third push-pull stage. This third stage consists of two inverting push-pull MOSFET switches in parallel with each other, effectively doubling the current. All connections are the same as with

the push-pull switches previously discussed, with the only difference being the direct parallel connection to the second push-pull switch. This final stage is necessary in order to ensure that the gate of the power MOSFET receives enough current to turn on. The final output of this stage is a positive pulse of approximately 15 V and 20 ns.

The final IRF510 power MOSFET phase produces the desired negative voltage pulse. Between this phase and the current boosting phase is a capacitor, which isolates the voltage pulse from the output of the previous stage and centers it around $-V_{CC}$, which has typically been set at -30 V for the recording of oscilloscope traces. $-V_{CC}$ is the gate voltage of the power MOSFET at all times except when the input signal has been carried through the pulser circuit and has passed through the capacitor. The capacitor is connected to the gate of the power MOSFET. The source of the power MOSFET is connected to the negative supply, $-V_{CC}$. It is also connected to the drain through a 100 kΩ resistor. The drain is connected through the output resistor, modeling an ultrasound transducer assumed to have an impedance of 50 Ω, to ground. It is the output of the drain that is considered the final output and has been measured as such. The final output of this phase, and the pulser as a whole, should be a negative voltage spike with a magnitude of $-V_{CC}$ and 30 ns. The final pulse depends upon the value chosen for $-V_{CC}$. In this case, the IRF510 is not rated for voltages over 100 V, and so $-V_{CC}$ should not surpass that value during testing, in order to protect the power MOSFET.

5.1.3. Soldered Digital Logic Circuit

Based upon the performance of the breadboarded circuit, it became clear that further optimization of the signal was necessary. It was posited that some of this optimization would result from constructing a soldered prototype. The soldered prototype circuit was laid out

identically to the breadboarded circuit and included single pin sockets to allow for ease of replacing the delay and load resistors. The ability to change the delay resistor was crucial, as the propagation time of the NAND chip was found to be greatly decreased upon measurement of the soldered prototype. Additionally, it was found that varying the value of this resistor would vary the final output pulse width, with a higher resistance corresponding to a longer pulse duration. An image of the current soldered prototype is shown below in Figure 10.

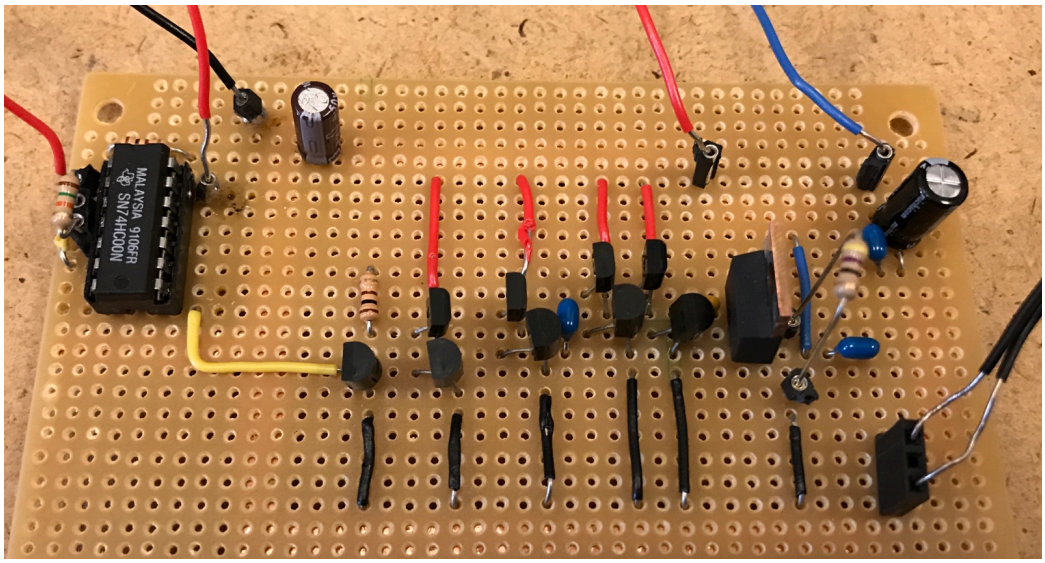

Figure 10: Soldered Digital Logic Circuit

The current soldered prototype was constructed using parts available within the ECBE department, so some will be replaced by the time the final design is implemented. The IRF510 power MOSFET will be replaced with the 201N09A power MOSFET in the final device. The other components will likely not be replaced, as they have been chosen for use in the final device. One major difference between the current model and the final model is the current prototype's reliance upon an external power supply. Since the final device will be self-contained, the high voltage supply will either be on board the board itself or contained within the device housing. Since a goal of the project is to implement it using a PCB, the final device will not be

constructed on a perfboard, and will likely look quite different. However, the general layout of the circuit and the various components, in a general sense, will be used in the final pulser design.

5.2. Receiver Design

During the Fall Term, designing the receiver circuitry was not a large focus, so there is not a great deal of information pertaining to this design. General research into its design and functionality has been conducted, however; and it has been determined that it will consist of the following stages: protection circuitry, a pre-amplification phase, and a final amplification phase, illustrated in the block diagram shown in Figure 11, below.

Figure 11: Block Diagram of Receiver Circuit

Specific parts have not yet been chosen, but aside from the protection circuitry, this design should not be immensely complicated or demanding. Svilainis and Dumbrava's circuit will be used in the preliminary design [4]. The most important factor of this design is ensuring that the protection circuitry is able to withstand the high power dissipation and isolate the high voltage signals from the more delicate receiver circuitry.

5.3. Overall Design

The overall design itself has not yet been considered, but research into various components that will affect the overall device has been conducted. Because of the choice of high-voltage power supply, the final enclosure will be quite large, as it must encompass both the wall-line module and the device. This will result in two separate power cables, one to power the

high-voltage supply, and one to power the device itself. Additionally, the final device must have a BNC connector for input/output and a BNC connector for external triggering. The goal of the project is still to make use of a PCB for the pulser/receiver circuitry and to enclose the entire device in a metal housing, making it appear similar to the industry standard machine.

6. PRELIMINARY TESTING RESULTS

Not every phase of the design process was fully tested, as modifications were made before oscilloscope traces were taken and saved. However, the key phases of the design tested are detailed below, as well as the justification for moving to the next phase of the project.

6.1. Brown and Lockwood's Design Results

The pulser circuit given in Brown and Lockwood's paper was simulated. The simulation schematic and the results of that simulation are shown below in Figures 12 and 13.

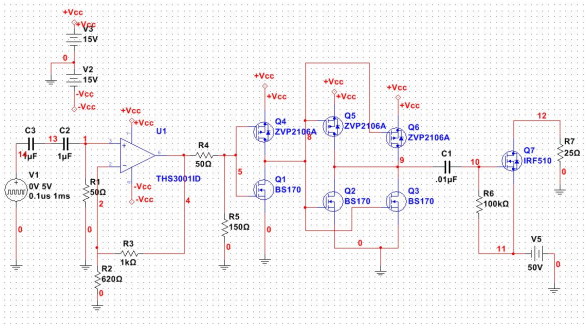

Figure 12: Schematic of Brown and Lockwood's Circuit

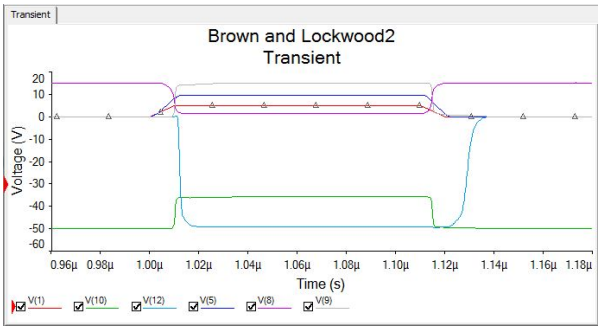

Figure 13: Simulation Results of Brown and Lockwood's Circuit

After the simulation worked reliably, a breadboarded prototype was built, replacing some of the higher-functioning, more expensive components mentioned with components already on hand in the ECBE Department, namely swapping the THS3001 op-amp for the LF356N and the 501N04A power MOSFET for the IRF510. No final output was ever attained from this prototype, but in observing the output of various stages, it was discovered that the width of the output pulse was directly related to the width of the input pulse. As Professor Buma desired a shorter output pulse width, some modification had to be made to the first phase of the pulser circuitry. The correlation between the input pulse width and the output pulse width was observed on the oscilloscope, but not permanently recorded. From this step, the first phase of the pulser circuitry, the pulse generator, was disassembled and a digital logic gate was implemented instead.

6.2. Breadboarded Logic Gate Design Results

The NAND gate pulse generator stage could take a signal of varying duration as its input, so long as the amplitude was around 5 volts. During testing, this stage took a positive 5 volt pulse of 10 μs as its input, and output a positive 5 volt pulse of varying signal width, depending upon the delay resistor, which was 30 kΩ for this testing phase. The output of the pulse generator phase is shown below in Figure 14. The signal out is approximately 6 V, and lasts for 130 ns.

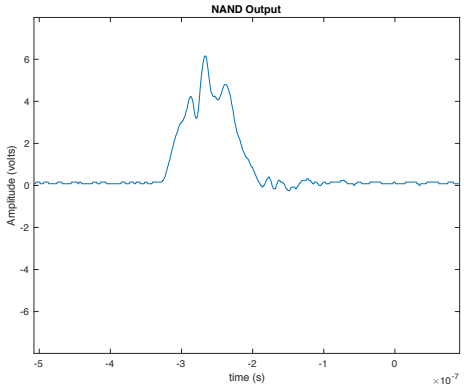

Figure 14: NAND Gate Pulse Generator Output Pulse

During the testing of this design, the need for a level shifter, used to increase the voltage from the 5 volts put out by the NAND gate to the 15 volts required to turn on the P-channel MOSFET, was discovered. This additional phase has already been incorporated into the block diagram of the pulser circuit from Figure 8. Figure 15, below, shows the output of this phase. The voltage of this pulse is approximately -15 V and the duration is 180 ns.

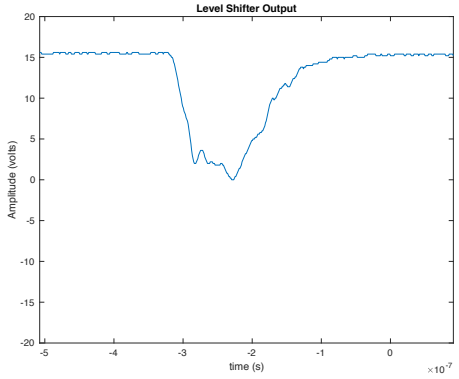

Figure 15: Level Shifter Output Pulse

Each of the two inverting push-pull stages works as desired, inverting the signal fed into it and providing further overall stability. The intermediate output of the two push-pull phases is a positive pulse of approximately 15 V and 140 ns. The final output of the push-pull phases is a negative pulse of approximately -15 V and 140 ns. The outputs of the first and second push-pull stages are shown below in Figures 16 and 17.

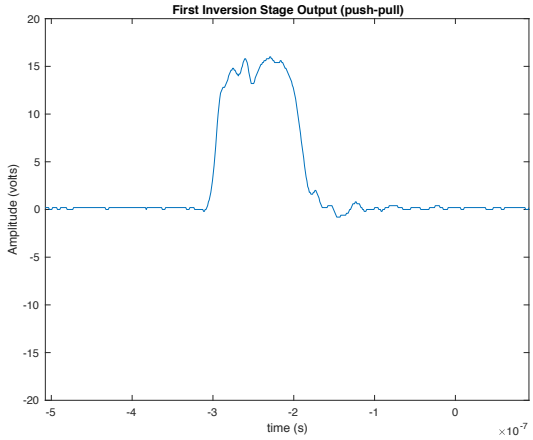

Figure 16: First Inversion Output Pulse

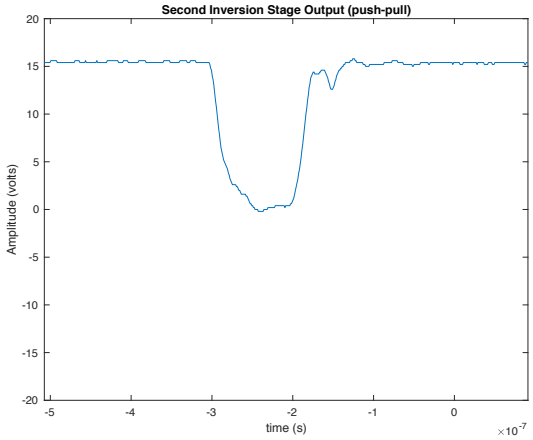

Figure 17: Second Inversion Output Pulse

The current boosting phase inverts the signal one last time so that the input to the power MOSFET is a positive voltage spike. The output of this final inversion stage is shown below in Figure 18, and the signal after it has been passed through the capacitor is shown in Figure 19. The final inversion stage has a positive pulse amplitude of approximately 15 V and 120 ns, and the signal after being passed through the capacitor is identical, but centered around -V_{CC}, -30 V.

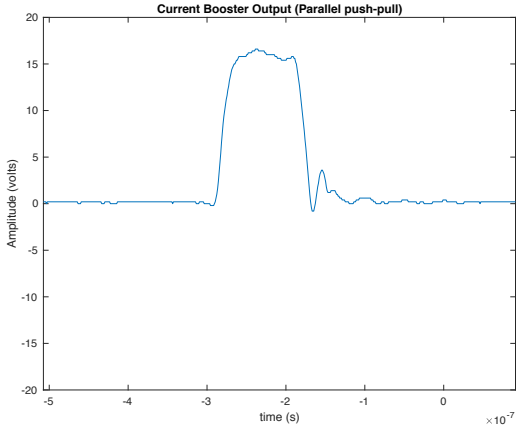

Figure 18: Current Booster Output Pulse

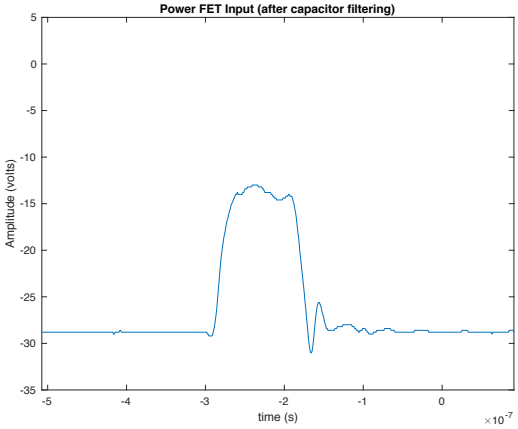

Figure 19: Power MOSEFT Input Pulse

The power MOSFET outputs a negative voltage spike whose highest magnitude is approximately equal to the negative voltage supplied to the source, $-V_{CC}$. This final output is shown below in Figure 20. The pulse width is approximately 120 ns, though it takes an additional 60 ns for the signal to return to 0 V.

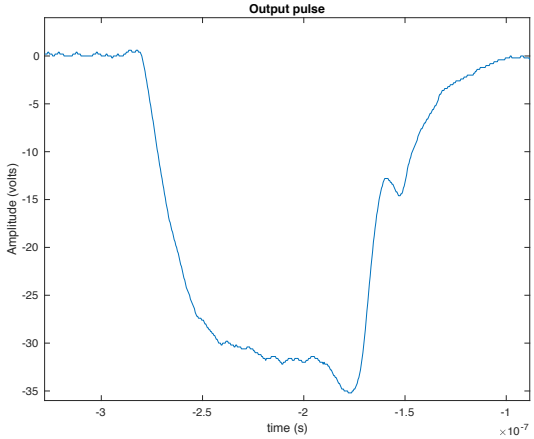

Figure 20: Final MOSEFT Output Pulse

6.3. Soldered Logic Gate Design Results

While attempting to find the appropriate delay resistor for the newly soldered circuit, it was discovered that varying this resistor value would correspondingly vary the output pulse width. An example of this is shown below in Figures 21 and 22. Figure 21 features a pulse of approximately 110 ns, and was taken using a 15 kΩ delay resistor. Figure 21 features a pulse of approximately 330 ns, and was taken using a 100 kΩ delay resistor.

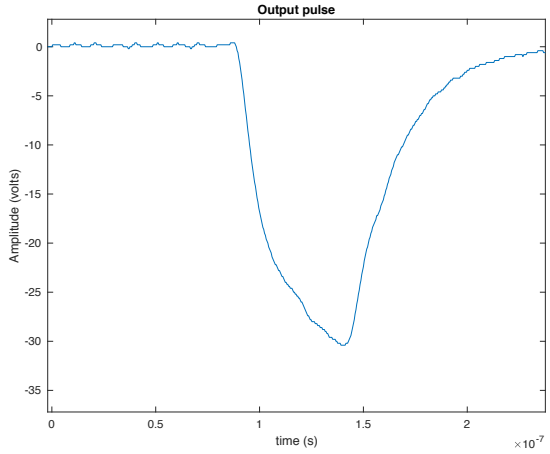

Figure 21: Short Final MOSEFT Output Pulse

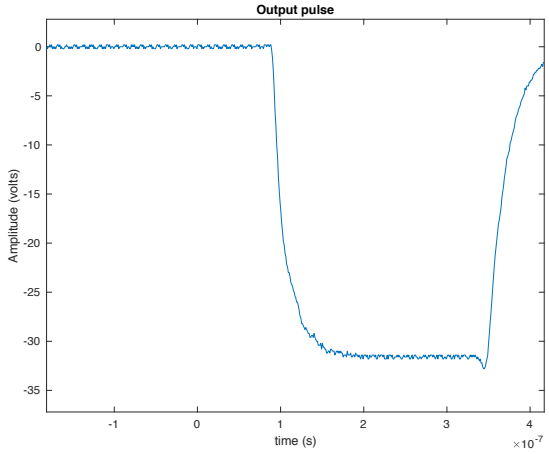

Figure 22: Long Final MOSEFT Output Pulse

The lowest resistor value that provided maximum pulse depth was found to be 15 kΩ. Except for Figure 22, all oscilloscope traces were taken using this 15 kΩ value. The soldered circuit on the whole provided a somewhat faster, more stable signal, but problems of optimization still remained. While the final pulse width was shorter than that of the breadboarded circuit, it was still longer than desired, and not as short as predicted. Part of this behavior could be attributed to the fact that the components used are not the optimal ones decided upon, the inherent delay of the function generator, or the delay associated with the act of taking a scope trace. Further pulse width optimization methods will be explored in the upcoming months.

Measurements were taken at the same places as the breadboarded circuit, and these outputs are shown below in Figures 23-28. The NAND output pulse is about 3 V and 80 ns, while the level shifter is about -15 V and 100 ns.

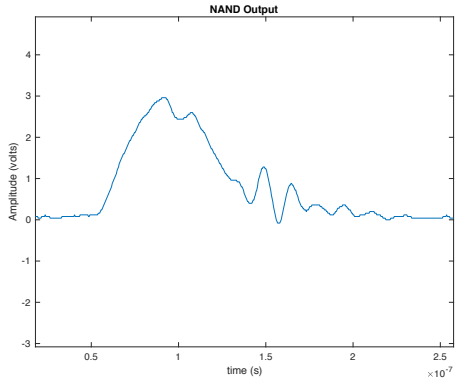

Figure 23: Soldered NAND Output Pulse

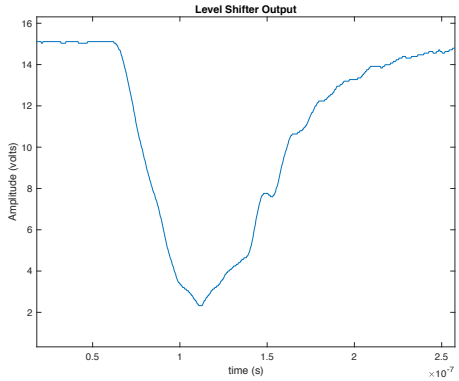

Figure 24: Soldered Level Shifter Output Pulse

The first inversion stage is about 13 V and 90 ns, and the second about -14 V and 90 ns.

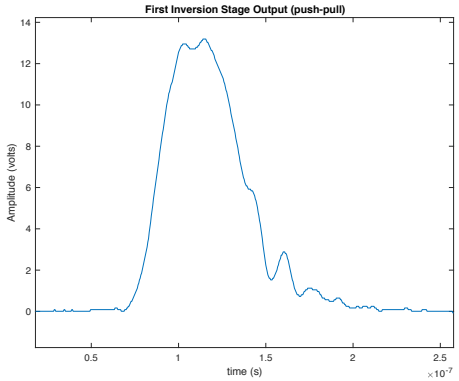

Figure 25: Soldered First Inversion Stage

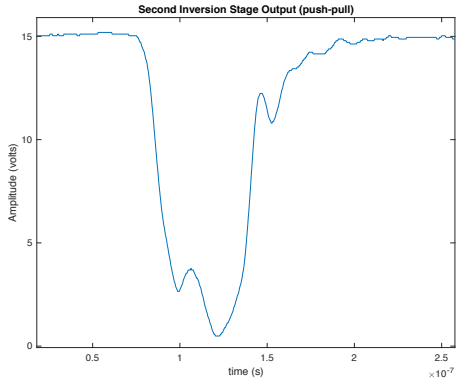

Figure 26: Soldered Second Inversion Stage

The current booster output is approximately 14 V and 90 ns. Again, the signal passed through the capacitor is identical, but it is centered around -29 V instead of 0.

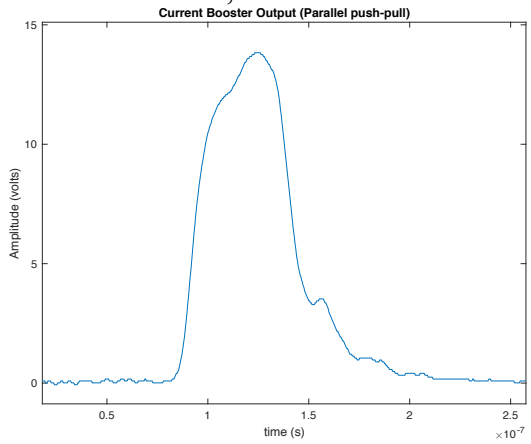

Figure 27: Soldered Current Booster Output

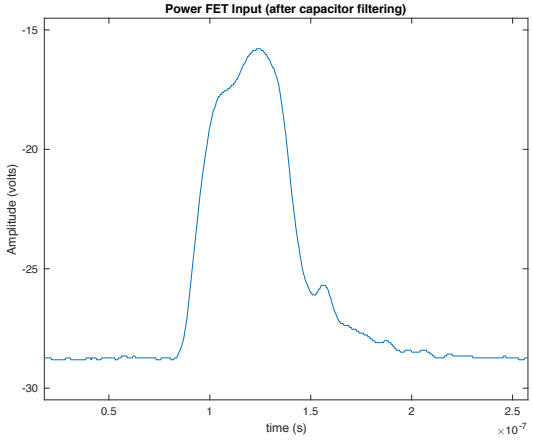

Figure 28: Soldered Power MOSEFT Input

Figure 21 already demonstrates the final output behavior of the soldered pulser circuit. There, the final voltage was approximately -30 V, and the final duration approximately 100 ns, with an additional 50 ns required for the signal to return to 0 V.

One final output test was conducted upon the soldered prototype, using the 15 kΩ delay resistor. $-V_{CC}$ was set at -60 V, and the output was measured, shown below in Figure 29. This high-voltage pulse was approximately - 59 V and 90 ns, though it took an additional 50 ns for the signal to return to 0 V. This high voltage pulse has the same shape and behavior as the lower voltage pulse, with the only difference being the amplitude of the pulse.

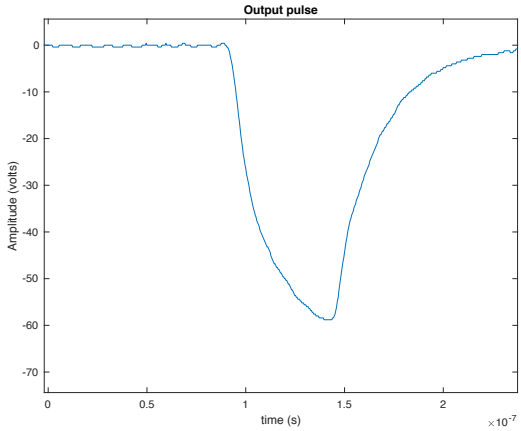

Figure 29: High Voltage Final MOSFET Output Pulse

7. IMPLEMENTATION SCHEDULE

The winter break will limit physical progress that can be made on the project, but a great deal of research and theoretical work can be completed in the upcoming time away from campus. Though the time away from the laboratory is not ideal, the winter break will be a good time to focus on some of the theoretical research necessary for future project success. The Winter Term will initially focus on finalizing the pulser circuit design and designing and testing the receiver circuit, as well as how to implement them together. From there, the overall device design will be considered. Final choices pertaining to the use of a PCB and the device housing will be made. More detailed scheduling information is included in the subsections below.

7.1. Implementation Schedule for Pulser Stage

The pulser prototype constructed from available parts is essentially functional, though a great deal of optimization is necessary. Some of this optimization might be attainable through the purchasing of higher-quality parts, but some of it is also dependent upon other factors. These factors were explored throughout the end of this term, so that the current pulser circuit prototype is as optimal as possible. The last few days of this term were focused on finalizing component choices and purchasing those necessary for the pulser circuitry. This purchasing deadline has been set so that upon return to school in Winter Term, the first week can be dedicated to the construction and testing of basic pulser prototype.

7.2. Implementation Schedule for Receiver Stage

Access to laboratory functions will be nonexistent over the winter break, but research will be conducted into at least two options for receiver circuitry, with plans to implement these designs immediately upon return to campus. The second week of Winter Term will be devoted to

constructing a prototype of the receiver circuitry using components available in the ECBE Department and purchasing additional components, if necessary. So long as the necessary components are obtained, the final prototype of the receiver circuitry should be completed by the end of the third week.

7.3. Implementation Schedule for Higher-Level Functions

Another research goal for the winter break is learning how to use the PCB design software Eagle and potentially choosing a PCB manufacturer. Eagle is free to download for students, so while laboratory access will be impossible, progress can be made in learning how to use PCB software and the design of the final PCB for the device. Beginning to design the PCB over the winter break also means that future functions can be added as needed, rather than having to devote a continuous period of time to the design of a PCB for the device during the term. Based upon the turnaround time of the PCB manufacturer, a final PCB design shall be sent off for printing with enough time to test and implement the PCB circuit before week six.

7.4. Implementation Schedule for Overall Device

Research into the wall line connection and high voltage power supply chosen at the end of this term will also be conducted over the winter break, so that theoretically, the only future work necessary to be done with these components is the actual implementation. As soon as the basic receiver design is finalized, the overall device will be put together using these components, and the basic functionality will be tested.

While this basic functionality testing is being conducted (or before, depending on the receiver design), the additional, desired input adjustments will be designed for, measured, and tested. As additional functions become practical to implement, their circuitry will be added to the

PCB design. By week six, whatever functions can be implemented on the PCB will be included in the final design. The PCB design will be finalized at this point, and the PCB itself will not be modified further. However, it will ideally be possible to leave the option for further input adjustments and customization open, so that any functions not implemented by this deadline can still be developed and included in the final device.

The final device housing will be put together after testing is conducted and completed on the finalized prototype of the pulser/receiver circuitry. While testing must be completed by week seven in order to have discussable results for the final presentation, the construction of the mounting hardware and housing can be completed during this final testing phase as well. In this way, the device itself should be mostly finished before the final presentations, requiring only small adjustments or aesthetic enhancements before the end of the term.

8. REFERENCES

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9. APPENDICES

The following pages feature appendices with the following information:

- **Appendix A:** Original SRG proposal (submitted Fall ’18)
- **Appendix B:** Notice of SRG Funding
- **Appendix C:** ECE-498 Poster from 11/1 Poster Session Week 9

Appendix A

Project Proposal
Andrea Huey

Introduction: Ultrasound imaging is a vital medical technology, as it allows professionals to get a closer look at the inside of what they are studying without actually having to open the person or object they are attempting to observe. While this variety allows people the ability to choose exactly what they want in a machine, many industry machines are designed with a great deal of adjustable features, and therefore cost a great deal of money. The primary goal of this project is to design a low-cost pulser/receiver. Some additional functionality is desired, and will be designed into the project, but the current plan is to have the main phase of the design completed by the end of fall term. The first half of winter term will entail adding optional features to the device, and the second half ensuring that the overall device is functional and presentable.

Proposed project: As mentioned above, this project involves creating a low-cost alternative to the over a thousand dollar machine Professor Buma has (and uses). The low cost aspect also means that should Professor Buma need more than one pulser, he does not have to purchase another expensive machine, rather; he can use another, simpler device. Designing this device will also allow me to work with a topic not covered in depth through any course here at Union. The majority of the project time will be spent working with the individual circuit elements, trying to build a functional prototype, but the desired finished project should be constructed on a Printed Circuit Board (PCB) and mounted in a metal enclosure, with appropriate BNC connectors to allow the device to be connected to coaxial cables and used just like the more expensive machine it is based on. An image of the original machine is shown below for reference, but my device will likely not look identical. Additionally, a rough sketch of the device in use is shown.

Figure 1: Image of Professor Buma's device

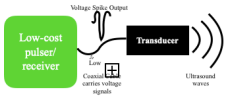

Figure 2: Sketch of key device stages

Design Requirements:
Output Requirements: The pulser shall produce a negative voltage spike around 180 volts (V) or greater, for 20 nanoseconds or less. A greater voltage spike, around 350 V, is more desirable, but 180 volts is a starting baseline. The repetition rate shall begin at 1 kilohertz (kHz), but can (and should) eventually be adjusted to go as high as 20 kHz. 5-10 kHz would be considered a more typical goal. The unit should also have two different trigger options; an internal trigger (that would keep time and self-trigger) and an external trigger (that would operate on a 0-5 volt logic scale and trigger due to an input signal to the device). Adjustability with regards to both the repetition rate and the triggers are longer term goals, but is desired.

Input Requirements: For initial testing, the load will be assumed to be 50 ohms. The receiver should be capable of measuring the pulse echo. One cable will be used both to transmit and receive, and as such, needs to be able to route a very high voltage signal and a very low voltage signal with no data loss at either extreme. The receiver circuitry would also need to be protected against the very high voltage pulse by using a duplexer and limiting diodes.

Cost Requirements: As the project is meant to be a cheaper alternative to Professor Buma's approximately $2,000 machine, the economic cost of this project is definitely a constraint. The design proposed in Brown and Lockwood's paper costs around $50, so the final circuit design, which would have more functionality than their proposed design, and include additional elements, would ideally be under $100, discounting the costs of the high voltage supply, the PCB, and the mounting hardware. More discussion of cost will be featured in the Budget section.

Electrical/Safety Requirements: The pulser/receiver shall run off the 120 volt wall line, and will be designed with those limitations in mind. It likely will not be used to take measurements on living beings, but it should be safe enough for such an eventuality. Because of the very high voltage, the system shall be designed with careful attention paid to the current running through components and the amount of power dissipated.

Size Requirements: The original machine is approximately 7 inches wide, 3.5 inches tall, and 9.1 inches deep, so my device should be no larger than those dimensions. Since this device will be a low-cost version, it should be even smaller than the more expensive machine. I do not yet have exact dimensions, as they will depend on the final circuit design and the size of the PCB and other components.

Design Approach: Much of the aesthetic elements of the project will be implemented during the winter term, after various sub-functions are confirmed to be working as expected. The goal for the end of the term is to have the pulser and receiver elements of the device functioning, and a preliminary design for the final device housing should be implemented. A high level block diagram of the key stages is shown below.

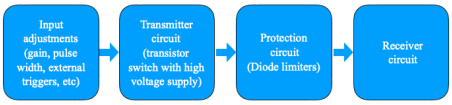

Figure 3: Overall Model of the Pulser/Receiver

The pulser will initially be tested alone. In order to do this, an oscilloscope probe can be used to measure the system output and display it on the oscilloscope. The output will be measured with and without a 50 Ω load. The voltage amplitude, duration of the pulse, and any pulse ringing will be the main aspects of the signal to observe.

The receiver will also be tested by itself before it is implemented with the pulser. A function generator will be used to model the input signal. Again, a scope probe will be used to measure the output of the receiver. In this case, the amplifier gain, frequency response, and noise will be the observed parts of the signal.

When both the pulser and receiver are tested together, the output (of the pulser)/input (of the receiver) cable will be connected to an ultrasound transducer. The transducer will then be placed in front of an acoustically reflective device, and a pulse will be sent. The final output of the receiver will be measured using an oscilloscope. Here, it is the peak frequency and bandwidth of the received pulse that will be measured.

These methods can be used to test each step of the device individually, but will also be used in the future to test the device when additional features are added. Assuming that a successful pulser/receiver is designed, the final result of those tests will be used as a benchmark for the device's future functionality, with appropriate scaling.

Anticipated Outcomes: The final device should behave comparably to the one Professor Buma is currently using. It should, at minimum, be able to send a very high voltage pulse (on the order of a hundred volts) to the ultrasound transducer and receive the very low voltage pulse (on the order of millivolts) sent back through the transducer. Additionally, some front-end adjustments will be implemented. These requirements include, but are not limited to, adjustable gain, adjustable pulse width, and adjustable gain, all of which should be able to be implemented with fairly simple circuit components. These components include variable resistors or capacitors, as well as regular resistors, capacitors, inductors, and other simple circuit components. Though the device may not be as finely tuned or accurate as the one Professor Buma currently uses, it should be able to be used for a rough estimation of the imaging work he is trying to accomplish.

Reason(s) Funding is Necessary: Funding is necessary for this project because I will need to be able to purchase key components, such as a high voltage supply, PCB materials, and mounting materials in order to successfully create and test the ultrasound pulser/receiver.

References:
[1] J. A. Brown and G. R. Lockwood, *A Low-Cost, High-Performance Pulse Generator for Ultrasound Imaging,* IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control., vol. 49, no. 6, June 2002.

[2] Olympus, "Manually Controlled Pulser- Receivers," 5072PR datasheet, 2009.

[3] J. K. Poulsen, *Low Loss Wideband Protection Circuit for High Frequency Ultrasound,* IEEE Ultrasonics Symposium, 1999.

Budget Breakdown: The components necessary to complete the device are broken down in the table below. The total amount requested is $399, with $362 going toward component purchase and $37 for shipping costs. The most expensive component is the high voltage supply, which is also the most necessary, due to the fact that the project features high voltage spikes. Many standard electrical components, such as resistors, transistors, and op-amps, can be found in the ECBE department, and so their cost is not included in the budget breakdown.

Table 1: Detailed Budget Breakdown

Item	Justification	Cost
Acopian Power Supply Model U400Y20	This high-voltage power supply can produce up to 400 volts. 400 volts is necessary to create a buffer for the maximum 350 volts Brown and Lockwood's circuit was designed for, though most of the testing will be conducted at a lower voltage. When using high voltage, care will be taken to ensure user safety.	$250
THS3001 Operational Amplifier	420 MHz current-feedback amplifier, used as a high input impedance line driver	*
3 VN2106 MOSFETs and 3 VP1304 MOSFETs	These MOSFETs are paired together (1 P-Type and 1 N-Type) to act as a push-pull switch.	*
501N04 Fast Power MOSFET	Used as a high power switch to turn the circuit on or off.	$27
2 50 Ω Resistors	Component in pulser circuit	*
150 Ω Resistor	Component in pulser circuit	*
1k Ω Resistor	Component in pulser circuit	*
25 Ω Resistor	Component in pulser circuit	*
100k Ω Resistor	Component in pulser circuit	*
620 Ω Resistor	Component in pulser circuit	*
2 1.0 µF Capacitor	Component in pulser circuit	*
0.01 µF Capacitor	Component in pulser circuit	*
2 BNC Connectors	Necessary to input/output voltage pulse and resultant signal, and to input external trigger	$11
Custom PCB Fabrication	Necessary for the final device to be neatly organized	$32
Mounting Hardware	Includes mounting enclosure, small metal sheets, screws, spacers, and washers	$42
Shipping Costs	Must pay for shipping for some specialty websites/companies	$37

* These components will be paid for by/are freely available in the ECBE department.

Appendix B

Dear Andrea Huey,

It is with pleasure that I am writing to inform you that the Student Research Grant Committee has approved a student research grant in the amount of $399.00 to enable you to carry out the project outlined on your application. ***Please read the following comments and directions carefully:***

The SRG Committee recommends funding of $399 for the purchase of materials related to your project. Please work directly with Lisa Galeo in the ECBE department to make the necessary purchases.

This grant is being made out of funds budgeted for the academic year 2018-2019. You may draw upon your SRG account through early May 2019 – **all spending must be completed by Friday, May 10, 2019 and receipts must be turned in by Tuesday, May 14, 2019.** You will be expected to spend these funds in general accord with the budget approved for your project.

Guidelines for spending your SRG funds can be found at:
http://muse.union.edu/undergraduate-research/student-research-grant-applications/

The Committee extends its best wishes for a successful project.

Sincerely,

Chad Orzel
Director of Undergraduate Research
Chair, SRG Committee

Cc: Prof. Chad Orzel (via separate email)
Advisor: Prof. Takashi Buma (via separate email)
Dept AA (for Reimbursements): Lisa Galeo (via separate email)

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Appendix C

Senior Project – Electrical Engineering and English Double Major – 2019

Designing a Low-Cost Ultrasound Pulser/Receiver

Andrea Huey
Advisor – Prof. Takashi Buma

Introduction:

- Ultrasound imaging is an incredibly powerful technology that grants the ability to see inside a patient or subject without cutting them open
- Ultrasound pulse transmitted by applying high voltage pulse to an ultrasound transducer
- Same transducer detects echoes, which are amplified to obtain data and reconstruct an image
- Commercial pulser/receivers can cost several thousand dollars
- Professor Buma needs a low-cost alternative so he can conduct experiments with multiple ultrasound transducers

Design Requirements:

- Pulser shall produce a -180 V spike, but should ultimately reach -350 V
- Duration of voltage spike should be <20 ns
- Initial repetition rate of 1 kHz, eventually shall be adjustable to 20 kHz
  - 5-10 kHz considered more attainable goal
- 2 different trigger options desired
  - Internal trigger that keeps time and self-triggers
  - Input trigger that operates on 0-5V logic scale
- Long term goals include repetition rate and trigger adjustability
- Most obvious requirement is cost since this is a a low-cost alternative

Preliminary Results:

- Designed and tested pulser circuit, working from preliminary circuit given in Jeremy A. Brown and Geoffrey R. Lockwood's paper

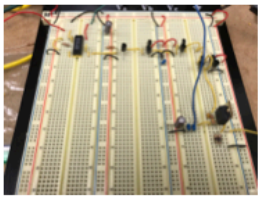

Figure 4: Breadboarded Pulser Circuit

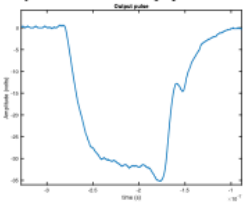

Figure 5: Final Circuit Output

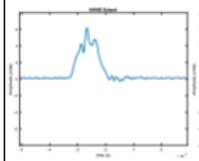

Figure 6: NAND Output

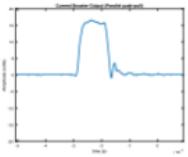

Figure 7: Current Booster Output

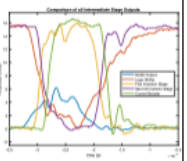

Figure 8: Multi Signal Comparison

- Final output pulse width is shorter than input stages, but is not yet at the desired pulse width of 20 nanoseconds
- Each stage has the general desired response, ignoring ripples
- Next step is soldering components and testing if that decreases pulse width and excess ringing/ripple
- Once pulser works as desired, begin designing/testing receiver

Preliminary Design:

- The pulser consists of four primary stages

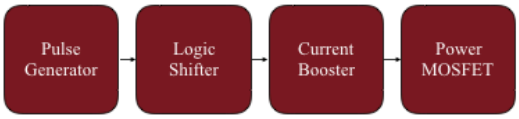

Figure 1: Block Diagram of Pulser Circuit

- Pulse Generator takes advantage of the inherent propagation delay in digital logic (NAND) to create a short pulse (~200 ns) from high input
  - In theory, this delay should be enough to produce the desired behavior, but a resistor was needed to further slow down the response
- Logic Shifter takes the final NAND output stage and the input value from +5V to +15V output in order to activate the CMOS inverter stages
  - This stage inverts the signal because it uses an n-channel MOSFET
- Two high-speed inverting CMOS inverter switch stages are needed to decrease the final pulse width even further
- Current Booster takes the output of the push-pull stages and increases the output current to drive the MOSFET gate capacitance
  - Current is increased because these are two push-pull stages in parallel
- Power MOSFET generates the very high voltage output pulse, but requires a lot of gate current to turn on quickly

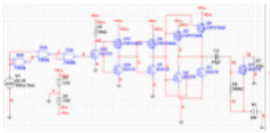

Figure 2: Pulser Circuit Schematic

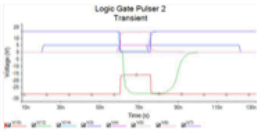

Figure 3: Pulser Circuit Outputs

- Circuit input is dark blue, final output is green
  - Pulse Generator output is purple, Logic Shifter output is light blue, Current Booster Output is pink, Power MOSFET input is red
  - Other lines are inverting push-pull stage outputs
- Note input pulse width compared to output pulse width
- Final output pulse width is wider than pulse width of inverting stages

Future Work:

- Finish testing the pulser output and solder an early prototype
- Design, test, and solder the receiver circuit
- Begin designing and testing adjustable input conditions
- Lay out components using a PCB software
- Design a case and housing for the final product
- Assemble the finished product

Acknowledgements:

- Thanks to Union College, Prof. Buma, SRG Funding, Gene Davison